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(54) Title of the Invention: Field-Effect Transistor

(57) [Abstract]

[Object] To provide a field-effect transistor (FET) which has an LDD structure, can reduce the increase in series resistance between a source and drain areas caused by an $n^-$ layer to a greater extent than a conventional FET and, has higher resistance to deterioration by hot carriers.

[Structure] A gate electrode 41 consists of the following three sections: a main gate section 41a made of a first material and two end gate sections 41b and 41c which are provided at both ends of the source and drain area sides of the gate section 41a and made of a second material. In addition, the first and second materials are selected so that the work function of the first material can become larger than that of the second material when the FET is of the n-channel type or

so that the work function of the first material can become smaller than that of the second material when the transistor is of the p-channel type.

[Claim(s)]

[Claim 1] A field-effect transistor characterized by having a gate electrode comprising the following three sections: a main gate section made of a first material and two end gate sections which are provided at both ends of the source and drain area sides of the gate section and made of a second material, wherein said first and second materials are selected so that the work function of the first material can become larger than that of the second material when the field effect transistor is of the n-channel type or so that the work function of the first material can become smaller than that of the second material when the field-effect transistor is of the p-channel type.

[Claim 2] The field-effect transistor of Claim 1, characterized by having a barrier layer for preventing a reaction between said main gate part and an edge gate sections when such a reaction occurs during heat treatment of the said first material and said second material.

[Claim 3] The field-effect transistor of Claim 1, wherein said first material and said second material are selected from the group consisting of $n^+$ polysilicon and $p^+$ polysilicon.

[Claim 4] The field-effect transistor of Claim 1, wherein said first material is selected from tungsten and said second material is selected from $n^+$ polysilicon or $p^+$ polysilicon.

[Claim 5] The field-effect transistor of Claim 1, wherein said first material is selected from a titanium nitride (TiN) and said second material is selected from $n^+$ polysilicon or $p^+$ polysilicon.

Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to field-effect transistors.

[0002]

[Description of the Prior Art] One type of a field-effect transistor is known as a MOS (Metal Oxide Semiconductor) type field-effect transistor (hereinafter referred to as a "MOSFET"). One type of such a MOSFET, which is a MOSFET having an LDD (Lightly Doped Drain) structure is disclosed, e.g., in IEDM Technical Digest, p.651, (1981). The explanation of this structure will be now given with reference to Fig. 5(A), which is a sectional view in the longitudinal direction of the gate of this LDD-type MOSFET.

[0003] In this MOSFET, the gate electrode 17 is formed on a silicon substrate 11 through a gate insulation film 15 in a predetermined position in the area surrounded by element isolation regions 13. Furthermore, sidewalls 19 are formed on the sides of source and drain regions of the gate electrode 17, respectively. Formed substantially below the aforementioned sidewalls 19 [a typo in the original where "17" is used instead of "19" -- tr. note] are $n^-$ layers 21, and respective source-drain regions 23 are formed sidewise of the $n^-$ layers 21 on the silicon substrate 11. The central portion that in Fig. 5(A) is designated by reference numeral 25 is an insulation film that during the manufacture of the aforementioned MOSFET structure is used as a mask.

[0004] Since in a vicinity of the drain region a MOSFET of such an LDD structure has a relatively small electromagnetic field in the transverse because of the presence of the $n^-$ layers 21 between the source-drain region 23 and the channel region (which is a part under the gate electrode 17 of the silicon substrate 11), the yield of hot carriers decreases compared with MOSFET of Fig. 5(B) that illustrates the most commonly used MOSFET of a single-drain structure. This significantly improves hot-carrier resistance.

[0005]
[Problem(s) to be Solved by the Invention] However, since a MOSFET of the LDD structure has low concentration of impurity in the layer 21, the series-resistance between the source region and the drain region becomes high and therefore reduces the drain current, which is undesirable.

[0006] Furthermore, since the above-described structure does not have the gate electrode above the $n^-$ layer 21, the carrier cannot be positively induced to the substrate part in which the layer 21 is formed. Therefore, the aforementioned series resistance cannot easily occur because the $n^-$ layer regions can be easily depleted by the traps and the interface levels generated by hot carrier impregnation.

[0007] Based on the above information, it is an object of the present invention to provide a field-effect transistor having the structure which is free of the above disadvantages.

[0008]
[Means for Solving the Problem] The above object is achieved by means of the present invention that provides a field-effect transistor characterized by having a gate electrode comprising the following three sections: a main gate section made of a first material and two end gate sections which are provided at both ends of the source and drain area sides of the gate section and made of a second material, wherein said first and second materials are selected so that the work function of the first material can become higher than that of the second material when the field effect transistor is of the n-channel type or so that the work function of the first material can become lower than that of the second material when the field-effect transistor is of the p-channel type.

[0009] In addition, according to the invention, the field-effect transistor is provided with a barrier layer for preventing a reaction between the main gate part and the end gate sections when such a reaction occurs during heat treatment of the first and second materials. It is understood that the aforementioned reaction results in the formation of a new substance that may cause diffusion of a part of one material into another and thus cause various phenomena that could impair the effect of the present invention. For example, the aforementioned reaction may include mutual diffusion of impurities when one of the aforementioned first and second materials is an $n^+$ polysilicon while the other is a $p^-$ polysilicon.

[0010]
[Function] The present invention makes it possible to obtain a field-effect transistor, where the gate electrode, i.e., an edge gate part, is formed on the substrate area which is equivalent to the region where $n^-$ layer is formed in the LDD structure. Since such a structure makes it possible to control the carrier density in the substrate region below such edge gate part by means of the edge gate part, it is easier to increase resistance in the region when the $n^-$ layer is formed. Thus, it becomes possible to alleviate solution of the prior-art problem associated with an increase of serial resistance in the LDD structures between the drain region and the source region.

[0011] Due to optimization of the working functions of structural materials from which the main gate region and the edge gate regions are made, the absolute value of the threshold voltage in the main gate part of the transistor becomes greater than the absolute value of the threshold voltage in an edge gate parts. Since in the present field-effect transistor a drain current does not flow until gate voltage becomes higher and the transistor part under the main gate region is turned on even if the transistor part under the edge gate part is turned on, the characteristics of the sub-threshold level is decided mainly by the transistor part under the main gate region. Finally, since the field-effect transistor of the aforementioned type is not affected even by deteriorations caused in the

substrate part under an edge gate electrode by the hot carriers, the transistor of the invention is to a lesser degree subject to fluctuations in the threshold voltage, sub-threshold level multiplier, $g_m$, or the like.

[0012]
[Practical Embodiments] Hereafter, the field-effect transistor of this invention will be considered by way of practical embodiments with reference to the accompanying drawings. In these drawings, the dimensions, shapes and relationships between various components of the transistor are shown schematically to the extent needed for understanding the principle of the invention.

[0013] 1. Explanation of the Structure

Figs. 1(A) and (B) are drawings used for explaining application of the invention to a MOSFET of an LDD structure. In particular, the structure shown in Fig. 1(A) relates to an embodiment that requires the use of a barrier layer 43 (which is described in more detail later) while the structure shown in Fig. 1(B) relates to an embodiment that does not require the use of the barrier layer 43. In all drawings, the MOSFETs of the embodiments are shown in cross-sections in the length direction of the gates. However, since middle insulator layers, contact holes, wirings, etc., are unnecessary for the explanation of this invention, illustration thereof are omitted.

[0014] In Figs. 1 (A) and (B), reference numeral 31 designates a semi-conductor substrate, 33 designates a field oxide film for separation of elements, 35 shows a gate insulation film, 37 is a source-drain region, 39 is a diffusion layer ($n^-$ layer) with impurity concentration lower than the source-drain region, and 41 is a gate electrode.

[0015] The above-described field-effect transistor has a gate electrode 41 that

consists of the following three sections: a main gate section 41a made of a first material and two end gate sections 41b and 41c which are provided at both ends of the source-drain area sides 37 of the gate section 41a and are made of a second material. In addition, the first and second materials are selected so that the work function of the first material can become higher than that of the second material when the FET is of the n-channel type or so that the work function of the first material can become lower than that of the second material when the transistor is of the p-channel type.

[0016] In Fig. 1(A), reference numerals 43 designates barrier layers used to prevent a reaction between the first material of the main gate part 41a and the second material of the edge gate sections when such a reaction occurs during heat treatment of the aforementioned first material and the second material. When the first and second materials are not subject to the above problems, the barrier layer 43 is not needed (see Fig. 1(B)). In Figs 1(A) and (B), reference numeral 45 designates an insulation layer that prevents penetration of ions into he main gate region 41a during ion implantation (including ion implantation during formation of $n^-$ layer in the LDD structure performed when the source-drain region is formed.

[0017] Here, the main gate part 41a is formed in the position that corresponds to the position of the gate electrode in the conventional LDD-type MOSFET, and the edge gate electrodes 41b and 41c are formed in the positions that in the conventional LDD-type MOSFET correspond to side walls and are made in the configurations as the sidewalls.

[0018] Moreover, the first material, which is the material for the main gate part 41a, and the second material, which is the material for the edge gate parts 41b and 41c, can be selected in compliance with the specific structural requirements. Examples of the first and second materials for field-effect transistors of an n-channel type and p-channel type, the working functions of these materials, and

examples of materials for barriers layers 43, when such layers are needed, are shown in Table 1 given below.

[0019]

[TABLE 1]

| Type of FET | Ex. No. | Working function and material of the main gate part | Working function and material of the edger gate parts | Material of the barrier layer |
|---|---|---|---|---|
| nMOS | 1 | $p^+$ polysilicon, about 5.2 eV | $n^+$ polysilicon, about 4.1 eV | $SiO_2$, SiON, SiN |
| | 2 | TiN (titanium nitride)*, about 4.7 eV | $n^+$ polysilicon, about 4.1 eV | Barrier layer is not needed |
| | 3 | W (tungsten), about 4.9 eV | $n^+$ polysilicon, about 4.1 eV | Tungsten nitride |
| pMos | 1` | $n^+$ polysilicon, about 4.1 eV | $p^+$ polysilicon, about 5.2 eV | $SiO_2$, SiON, SiN |
| | 2 | TiN (titanium nitride)*, about 4.7 eV | $p^+$ polysilicon, about 5.2 eV | Barrier layer is not needed |
| | 3 | W (tungsten), about 4.9 eV | $p^+$ polysilicon, about 5.2 eV | Tungsten nitride |

*[Typo in the Japanese original where tantalum nitride is mentioned in the parenthesis instead of titanium nitride - translator's note]

[0020] it can be seen from Table 1 that in the case of Example 1, the $SiO_2$ films, silicon nitride oxide (SiON) films, and silicon nitride (SiN) films protect $n^+$ polysilicon and $p^+$ polysilicon from mutual diffusion of impurities for both nMOS and pMOS type transistors. Furthermore, in the case of nMOS of Example 3 and pMOS of Example 3, a reaction between tungsten and polysilicon with the formation of tungsten silicide is prevented by the barrier layers made from the tungsten nitride.

[0021] 2. Explanation of the Manufacturing Process

For better understanding the present invention, let us consider an example of manufacturing a field-effect transistor of the invention with reference to the embodiment of the transistor of nMOS type shown in Fig. 1(A) and mentioned in Example 1 of Table 1. The sequential manufacturing steps will be explained with reference to Figs. 2 to 4. In all the drawings the transistors are shown in cross sections that correspond to the positions of the elements in Fig. 1.

[0022] First, the field oxide films 33 are formed on a silicon substrate 31 by a well-known method. Next, the gate insulation film 35 having a thickness of about 10 nm is formed on this silicon substrate 31, e.g., by thermal oxidation (Fig. 2(A)).

[0023] In the next step, in order to provide the MOSFET with a predetermined value of the threshold voltage, a channel region (not shown) is formed by implanting, e.g., boron (B) in the dose of $1.4 \times 10^{-12}$ $cm^{-2}$ and with the energy of 10 KeV into the silicon substrate 31 through the gate insulation film 35.

[0024] Next, in order to form a thin film for the main gate part 41a (see Fig. 1) of the gate electrode 41, a polysilicon (polycrystalline silicon) film having a thickness of about 300 nm is formed on the silicon substrate 31 by the low voltage chemical-vapor-deposition method (LPCVD method) that accomplishes formation of the aforementioned channel region. Then, in order to reduce resistance of the polysilicon film and to set a work function at a predetermined value, boron fluoride (BF2) is implanted into the polysilicon film with the dose of $1.0 \times 10^{15}$ $cm^{-2}$ with the energy of 70KeV. As a result, a $p^+$ type polysilicon film 41x having a work function of about 5.2eV is obtained above the silicon substrate 31 (Fig. 3(C)).

[0025] In the following stage, in order to form the mask for ion implantation, a silicon oxide film (not shown) is formed over the entire upper surface of the sample by a CVD method. A resist pattern (not shown) is formed as a mask for patterning the aforementioned $p^+$ type polysilicon film 41x to the configuration of the main gate part 41a (Fig. 1 ). The unnecessary portions of the silicon oxide film and the p+ polysilicon film 41x are removed by etching, whereby the respective main gate part 41a and the insulation film 4 as a mask for ion implantation are formed (Fig. 3(A)).

[0026] Now, in order to buffer the transverse electromagnetic field in the vicinity of the drain, an impurity, e.g., phosphorus (P) is implanted into the silicon substrate 31 in the dose of $1.0 \times 10^{12}$ with the energy of 30 KeV. This results in the formation of an $n^-$ layer 39 in the portions of the silicon substrate on both sides of the main gate portion 41a (Fig. 3(A)).

[0027] Next, $SiO_2$ films (Fig. 3(B)) are formed as the barrier layers 43 on the side walls of the main gate part 41 as oxide films obtained by thermal oxidation on both side surfaces of the main gate portion 41a. The processing atmosphere that may be used in the formation of the aforementioned $SiO_2$ films may comprise, e.g., gaseous nitride suboxide ($N_2O$) or ammonia ($NH_3$), wherein the sample is heat treated, e.g., by the RTA (Rapid Thermal Annealing) method with appropriate adjustment of the processing time for forming the barrier layers 43 by converting the $SiO_2$ film into a SiON film. Such a system prevents mutual diffusion of impurities between the $p^+$ polysilicon as a structural material of the main gate part and the $n^+$ polysilicon as a structural material of the edge gate parts.

[0028] The next step is formation of 300 nm-thick polysilicon films 41y (Fig. 3(C)) on the sample by the LPCVD method for forming edge gate parts 41b and 41c (Fig. 1).

[0029] Next, the unnecessary portions of the polysilicon film 41y are removed by reactive etching whereby sidewalls 41z [there is a typo in the Japanese original where reference numerals 43z are used instead of 41z – tr. note] made from a polysilicon film are formed on the barrier layers 43 located on the opposite sides of the main gate part 41 (Fig. 4(A)). Each such sidewall 41a has a thickness W (Fig. 4(A)) equal to 200 nm.

[0030] In the case of the specific sample of the present embodiment, arsenic (As) was implanted [into the silicon substrate through the insulation layer] with the dose of $1.0 \times 10^{16} cm^{-2}$ and with the energy of 40KeV(s). The implantation made it possible to form the source-drain region 37. Since the side walls 41z were also doped with arsenic, these side walls were turned into $n^+$ type polysilicon films with the working function of about 4.1eV, and the edge gate parts 41b and 41c could be formed (Fig. 4(B)).

[0031] In the following step, an insulator layers 51 (which are omitted from Fig. 1), such as PSG (Phosphor Silicate Glass) films or BPSG (Boro-Phosphor Silicate Glass) films are formed as an intermediate insulation films, e.g., by a CVD method over the entire surface of the sample, and then heat treatment is carried out for impurity activation of the source-drain region 37 (Fig. 4(C)).

[0032] Contact holes (not shown) are then formed in the intermediate insulation film, and wiring is carried out for a source electrode, drain electrode, and other components. Since after completion of the process shown in Fig. 4(C) the barrier layers 43 act as insulation, the main gate part 41a and the edge gate parts 41b and 41c are separately connected in the process which forms contact holes and wiring. At this stage the manufacturing of the field-effect transistor of the embodiment shown in Fig. 1 is completed.

[0033] The MOSFET of the other types presented in Table 1 can be easily manufactured by a process which will be further explained with reference to Figs. 2 to 4.

[0034] For instance, pMOS of Example 1 mentioned in Table 1 can be formed as shown in Figs. 2 to 4 by using an impurity of the opposite conductivity type and by performing ion implantation under predetermined conditions.

[0035] When the main gate part 41a of Table 1 is made from a tungsten, the process may be carried out in the same manner as described above with reference to Figs. 2 to 4, except that a tungsten film is formed by an appropriate method, e.g., by sputtering. In this case, the etching conditions should be set up for higher selectivity of etching tungsten and silicon oxide film so as not to etch the gate insulation film 35 which constitutes a sublayer in patterning the tungsten film to the shape of the main gate portion 41a. Furthermore, when tungsten nitride is used as the barrier layer 43, formation thereof can be carried out by heat treating the tungsten layer patterned to the shape of the main gate part 41a for about 30 min. at a temperature of 850°C in the atmosphere of gaseous ammonia, e.g., by the RTA method.

[0036] When the main gate part 41a of Table 1 is made from TiN, the process may be carried out in the same manner as described above with reference to Figs. 2 to 4, except that a TiN film is formed by an appropriate method, e.g., by sputtering. Since in this case the TiN film, which is the material of the main gate portion 41a, does not react with the $n^+$ or $p^+$ silicon, which is the material for the edge gate parts 41b, 41c, the step of the formation of the barrier layers 43 becomes unnecessary. In this case, the etching conditions should be set up for higher selectivity of etching the TiN film and silicon oxide film so as not to etch the gate insulation film 35 which constitutes a sublayer in patterning the TiN film to the shape of the main gate portion 41a.

[0037] Although the invention has been described with reference to specific embodiments of the field-effect transistors, it is understood that the invention is not limited only by these embodiments.

[0038] For example, the above embodiments showed application of the invention to MOSFETs of the LDD structure. However, the invention is also applicable to the structures without the low-impurity-concentration layer 39 in the substrate area under the edge gate electrode 41b and 41c.

[0039] Moreover, the main gate part 41a, the edge gate parts 41b and 41c, and the barrier layer 43 can be made from materials other than those described above and the working functions of these materials also can be changed, provided that the new materials and their functions do not go beyond the scope of the invention.

[0040] Moreover, the manufacturing steps were shown merely as illustration. Therefore, the field-effect transistor of this invention is not limited by the above-described manufacturing steps.

[0041]
[Effect of the Invention] As follow from the above description, the invention is efficient in that the gate electrodes, i.e., the edge gate parts, are formed in the LDD structure also in the areas of the substrate that correspond to the regions where the $n^-$ layers are to be formed, and this allows control of carrier density in the substrate regions under the edge gate parts by means of the latter. Since the increase in the resistance of the parts where $n^-$ layers are formed is reduced, it becomes possible to alleviate the problem of the prior art in connection with the increase of the series resistance that in the LDD structures occurs between the source region and the drain region.

[0042] Moreover, since in the field effect transistor of the invention the work functions of the materials of the main gate part and the edge gate parts are optimized, even if the transistor part under the edge gate part is turned on, the drain current will not flow until gate voltage set high and the transistor part under the main gate part is turned on. For this reason, sub-threshold level characteristics are decided mainly by the transistor part under the main gate part. Finally, the performance of the field effect transistor of the present invention is not affected even by some deterioration of the substrate areas under the edge gate electrodes caused by the hot carriers. Therefore, the transistor is subject to fluctuations in the threshold voltage, sub-threshold level multiplier, $g_m$, etc. to a lesser degree than the similar transistor of the prior art.

[Brief Description of the Drawings]

Figs. 1 (A) and (B) are sectional views of the field-effect transistors according to the embodiments of the invention.

Figs. 2 (A) - (C) are views that illustrate an example of manufacturing steps of the transistor of Fig. 1.

Figs. 3 (A) - (C) are views that illustrate further steps in manufacturing the transistor after the steps of Fig. 2.

Figs. 4 (A) - (C) are views that illustrate further steps in manufacturing the transistor after the steps of Fig. 3.

Figs. 5 (A) and (B) are views that illustrate manufacturing of the conventional field effect transistor.

[Description of Reference Numerals used in the Specification]

31: Semi-conductor substrate

33: Field oxide

35: Gate insulation film

37: Source-drain region

39: Low-impurity-concentration layer

41: Gate electrode

41a: Main gate part

41b, 41c: Edge gate parts

43: Barrier layer

45: Insulation layer

41x: $p^+$ polysilicon

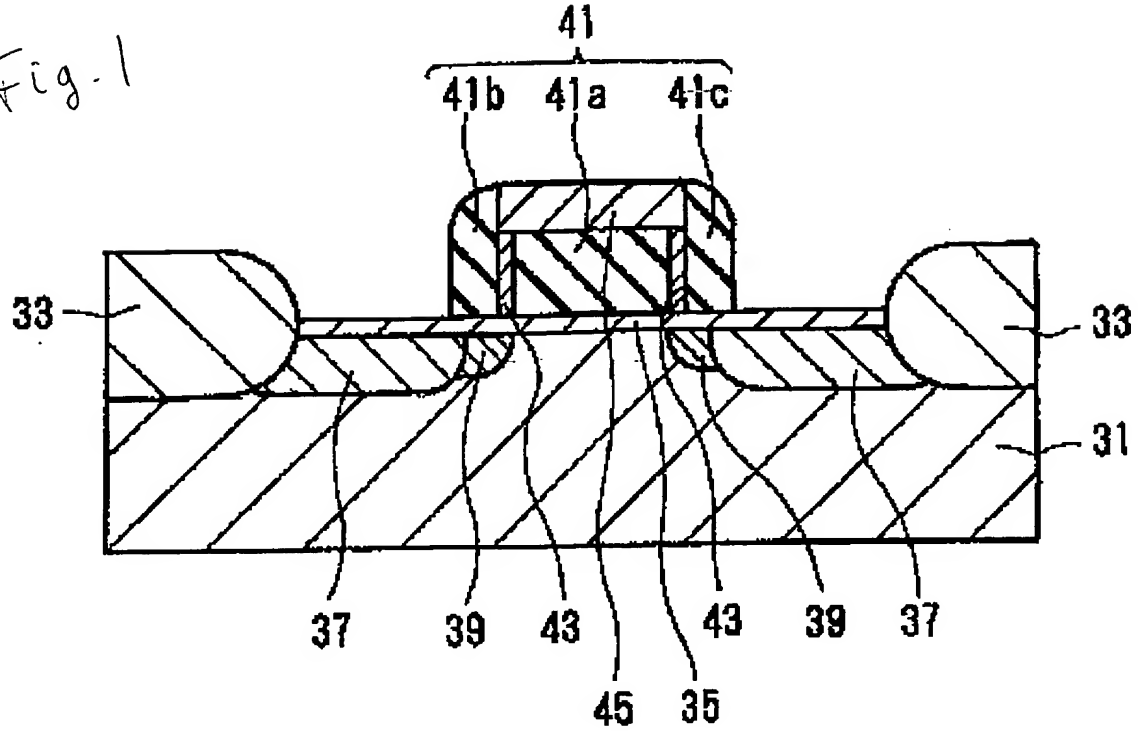
41y: Polysilicon

41z: Sidewall

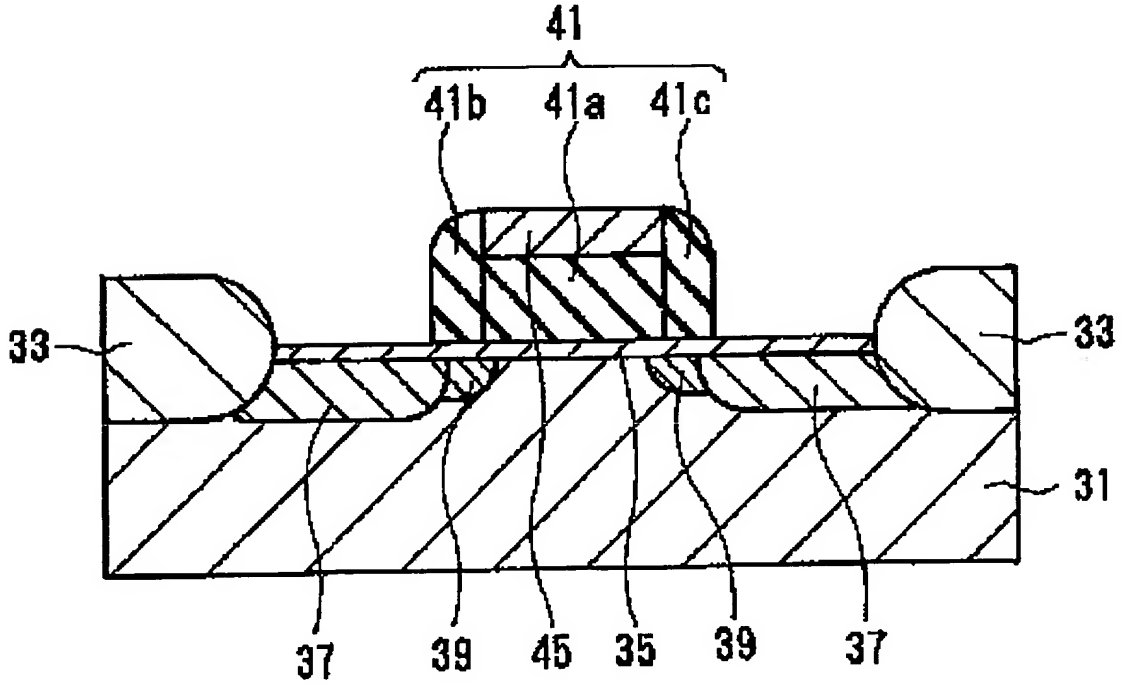
51: Insulation layer (intermediate insulation layer)

Fig. 1

(A)



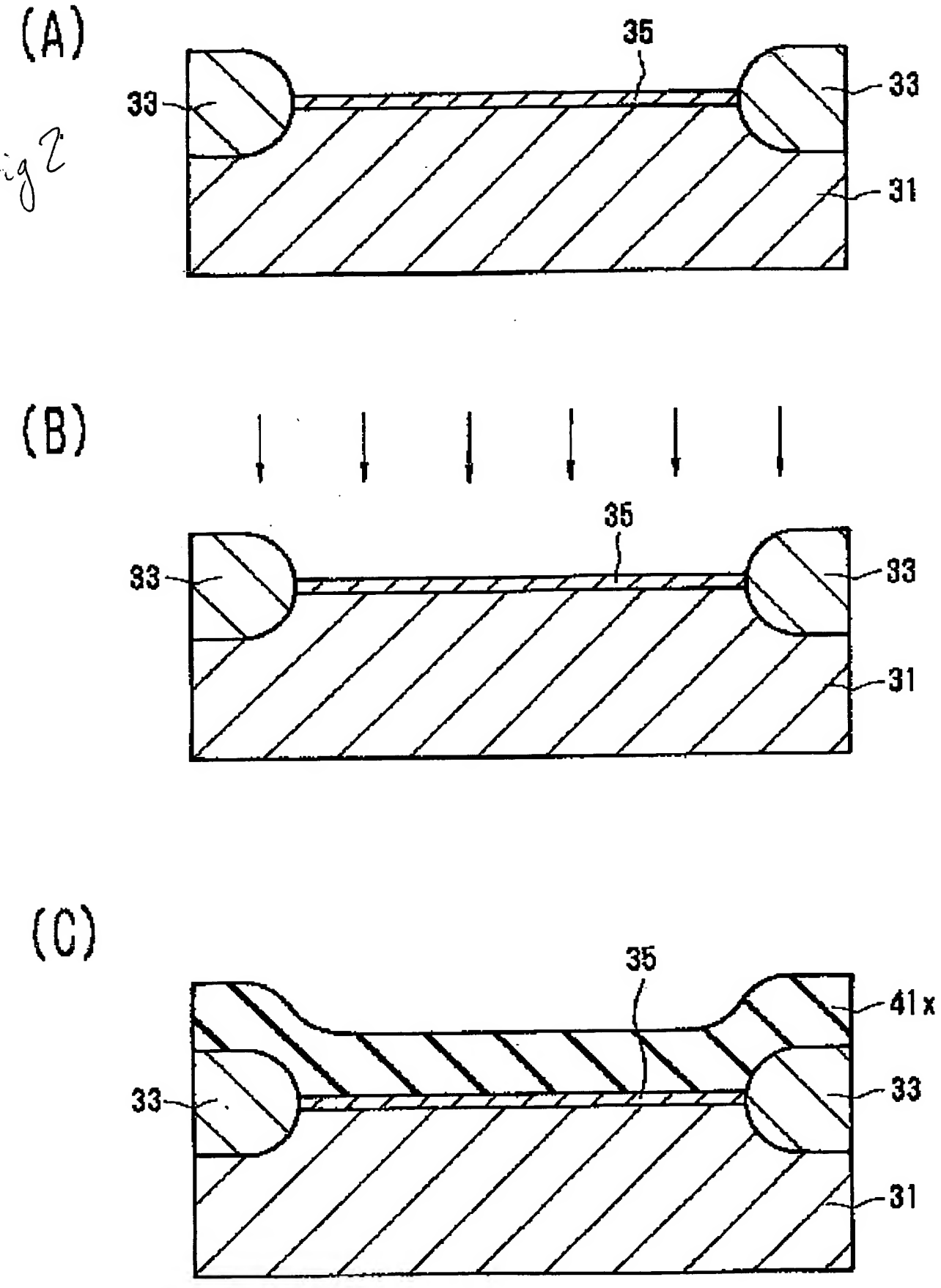

(B)




31 ：半導体基板
35 ：ゲート絶縁膜
39 ：低不純物濃度層
41a：主ゲート部分
43 ：阻止層
33 ：フィールド酸化膜
37 ：ソース・ドレイン領域
41 ：ゲート電極
41b, 41c：端部ゲート部分
45 ：絶縁膜

実施例の電界効果トランジスタを示した断面図

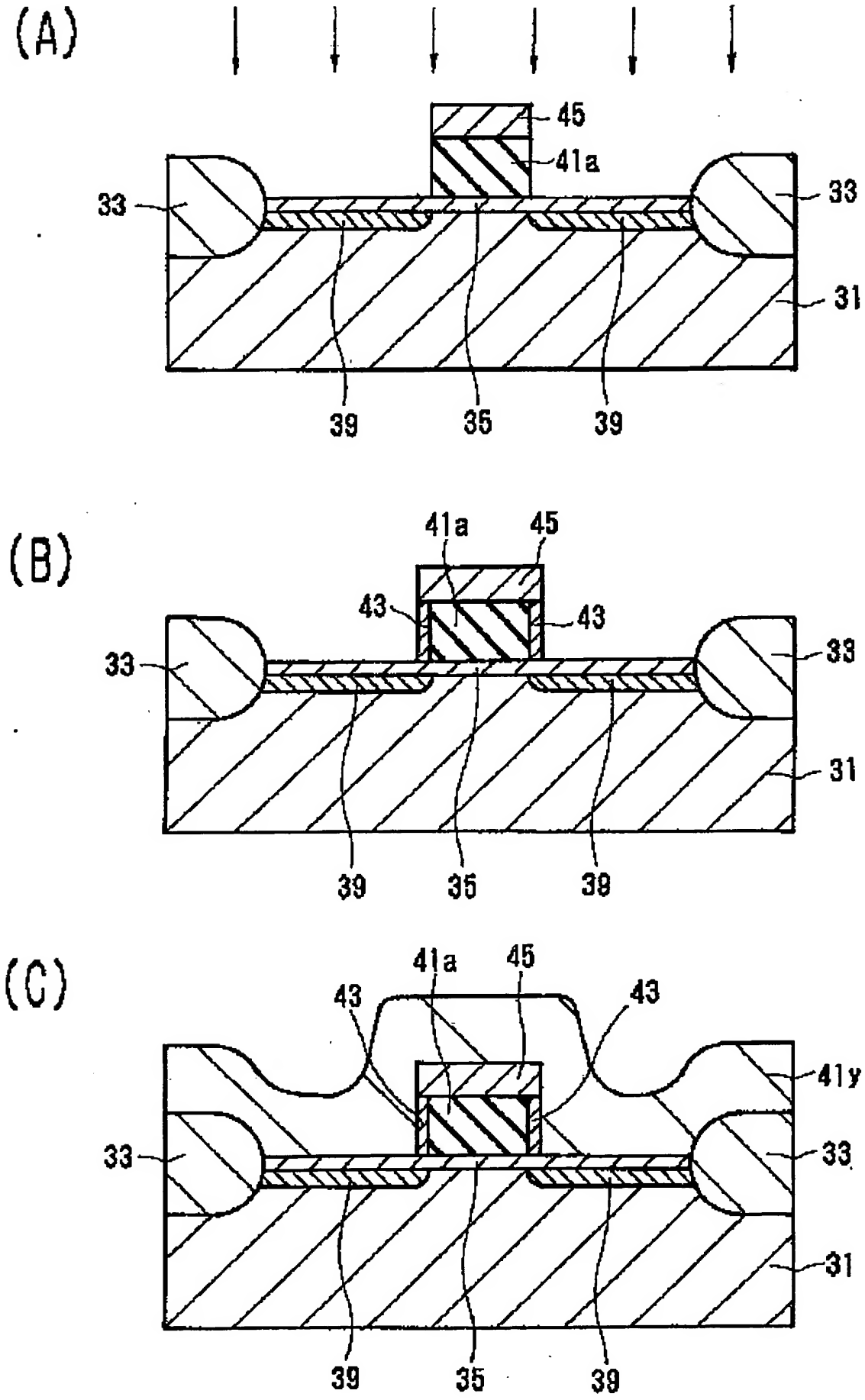
Fig 2




41x：$p^+$ ポリシリコン膜

実施例のＦＥＴの製法例を示した工程図（その１）

Fig 3

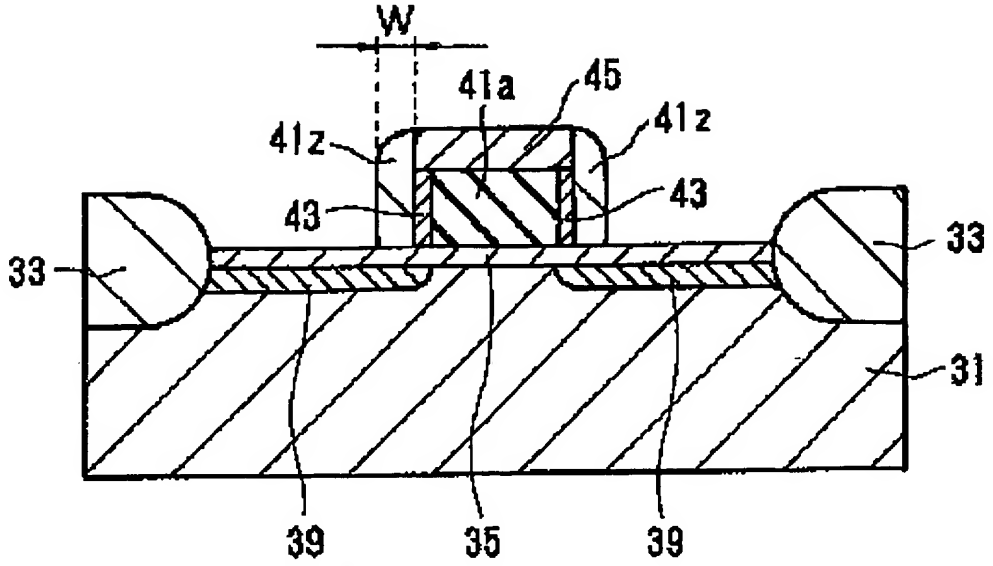



41y：ポリシリコン膜

実施例のＦＥＴの製法例を示した工程図（その２）

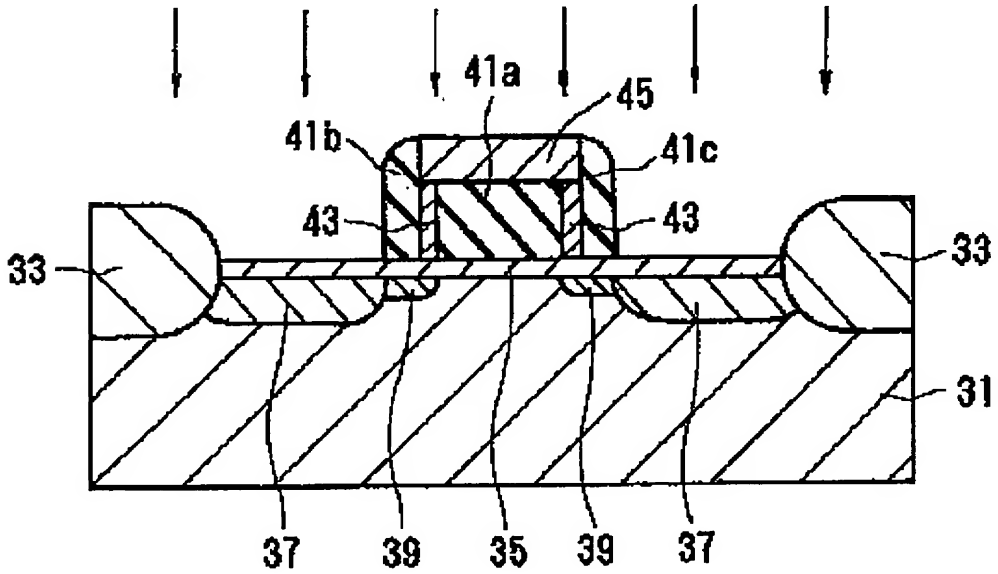
Fig-4

(A)




41z：サイドウォール

(B)

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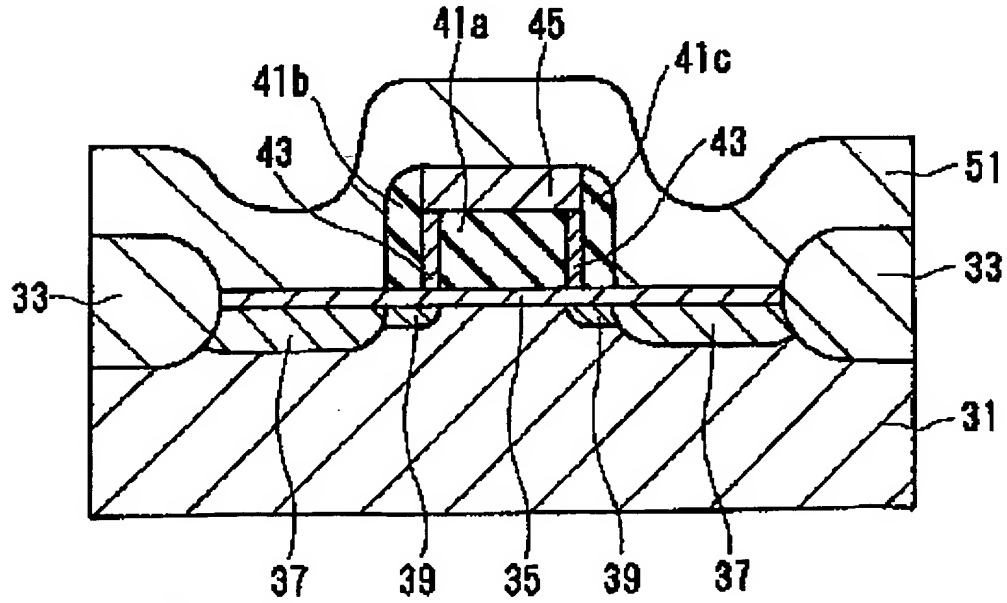
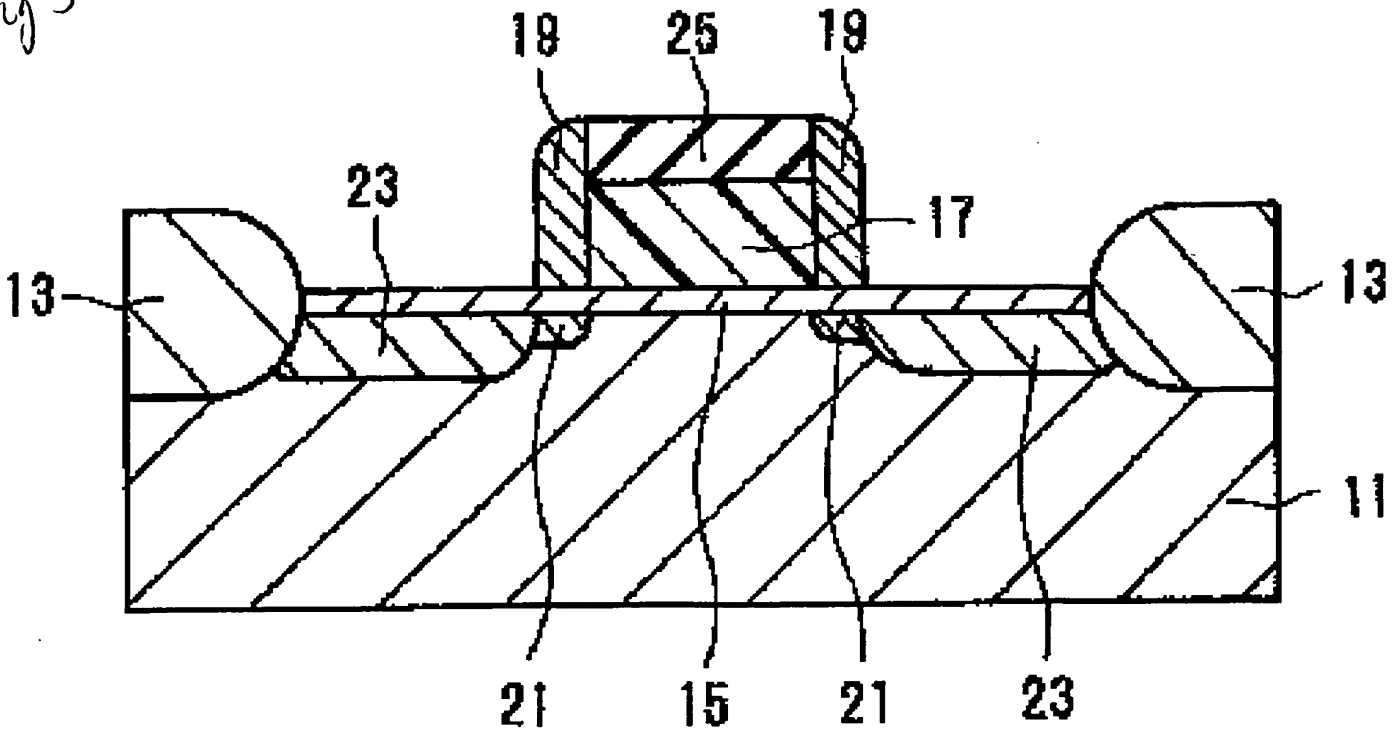



51：絶縁膜

実施例の製造例を示した図

Fig 5

(A)

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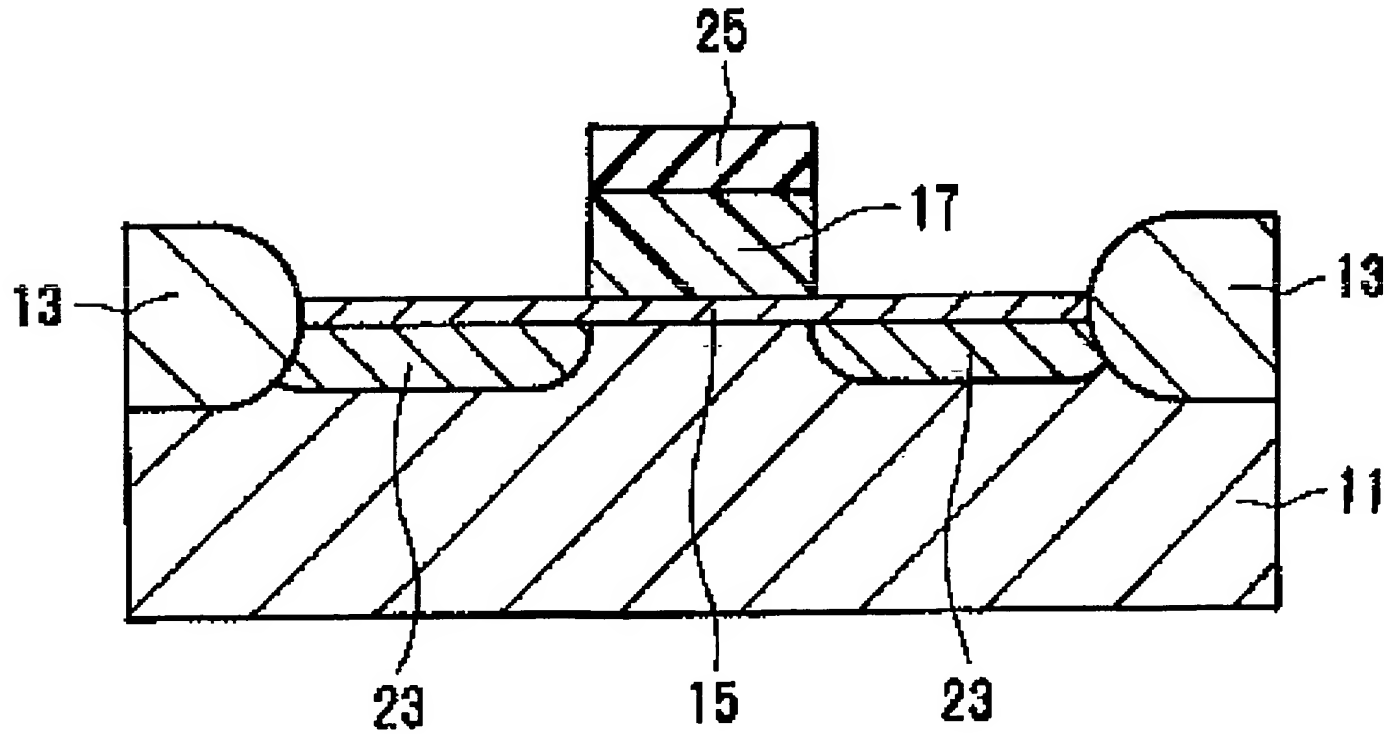


従来技術の説明に供する図